AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

The present invention provides a segmented correction apparatus that keeps the correction information for a speculative call/return instruction in different segments depending upon the location of the call/return within the pipeline, thereby enabling selective correction based on the stage in which the call/return instruction resides at the time of the detection of the invalidating event relative to the stage that detects the invalidating event. In one aspect the present invention provides an apparatus for correcting a call/return stack in a pipelined microprocessor. The apparatus includes a first stack, having a first plurality of entries for storing correction information related to call or return instructions present in a first plurality of stages of the microprocessor pipeline. The apparatus also includes a second stack, coupled to the first stack, having a second plurality of entries for storing correction information related to call or return instructions present in a second plurality of stages of the microprocessor pipeline. The apparatus also includes control logic, coupled to the first and second stacks, for receiving a first control signal indicating a call or return instruction is passing from the first plurality of stages to the second plurality of stages. The control logic moves the correction information associated with the call or return instruction from the first stack to the second stack in response to the first control signal. The apparatus also includes a second control signal, received by the control logic, for indicating the call or return instructions present in the first plurality of pipeline stages were speculatively incorrectly executed. The control logic corrects the call/return stack using the correction information stored in the first plurality of entries of the first stack, in response to the second control signal. The apparatus also includes a third control signal, received by the control logic, for indicating the call or return instructions present in the first and second plurality of pipeline stages were speculatively incorrectly executed. The third control signal indicates

an instruction preceding the call or return instructions present in the first and second plurality of pipeline stages generated a microprocessor exception.

In another aspect, the present invention provides a method for maintaining consistency between a call/return stack (CRS) in a pipelined microprocessor and a memory coupled thereto. The method includes receiving requests to update the CRS in response to a presence of call or return instructions. The method also includes storing correction information into a first buffer, in response to the receiving. The method also includes detecting a condition in which one of the call or return instructions has proceeded past a first stage of the microprocessor pipeline configured to detect a branch instruction misprediction, after the storing. The method also includes moving a portion of the correction information from the first buffer to a second buffer, in response to the detecting. The invalidating event comprises an exception. The method further includes correcting the CRS with the correction information stored in the first buffer if the first stage detects the invalidating event and correcting the CRS with the correction information stored in the first and second buffer if a second stage of the microprocessor pipeline detects a second invalidating event. The second stage is below the first stage.

In another aspect, the present invention provides a computer program product for use with a computing device, the computer program product having a computer usable storage medium having computer-readable program code embodied in the medium for providing an apparatus for correcting a call/return stack in a pipelined microprocessor. The program code includes first program code for providing a first stack having a first plurality of entries for storing correction information related to call or return instructions present in a first plurality of stages of the microprocessor pipeline. The program code also includes second program code for providing a second stack, coupled to the first stack, having a second plurality of entries for storing correction information related to call or return instructions present in a second plurality of stages of the microprocessor pipeline. The program code also includes third program code for providing control logic, coupled to the first and second stacks, for receiving a first control signal indicating a call or return instruction is passing from the first plurality of stages to the second plurality of

stages. The control logic moves the correction information associated with the call or return instruction from the first stack to the second stack in response to the first control signal. The program code also includes fourth program code for providing a second control signal, received by the control logic, for indicating the call or return instructions present in the first plurality of pipeline stages were speculatively incorrectly executed. The control logic corrects the call/return stack using the correction information stored in the first plurality of entries of the first stack, in response to the second control signal. The program code also includes fifth program code for providing a third control signal, received by the control logic, for indicating the call or return instructions present in the first and second plurality of pipeline stages were speculatively incorrectly executed. The third control signal indicates an instruction preceding the call or return instructions present in the first and second plurality of pipeline stages generated a microprocessor exception.

In another aspect, the present invention provides an apparatus for correcting a call/return stack in a pipelined microprocessor. The apparatus includes a first stack comprising a first plurality of entries for storing correction information related to call or return instructions present in a first plurality of stages of the microprocessor pipeline. The apparatus also includes a second stack, coupled to the first stack, comprising a second plurality of entries for storing correction information related to call or return instructions present in a second plurality of stages of the microprocessor pipeline. The apparatus also includes control logic, coupled to the first and second stacks, for receiving a first control signal indicating a call or return instruction is passing from the first plurality of stages to the second plurality of stages. The control logic moves the correction information associated with the call or return instruction from the first stack to the second stack in response to the first control signal. The apparatus also includes a second control signal, received by the control logic, for indicating the call or return instructions present in the first plurality of pipeline stages were speculatively incorrectly executed. The control logic corrects the call/return stack using the correction information stored in the first plurality of entries of the first stack, in response to the second control signal. The apparatus also includes a third control signal, received by the control logic, for indicating

the call or return instructions present in the first and second plurality of pipeline stages were speculatively incorrectly executed. The control logic corrects the call/return stack using the correction information stored in the first and second plurality of entries of the first and second stacks, in response to the third control signal. For each valid one of the first plurality of entries, the control logic pops the top valid one of the first plurality of entries from the first stack, and corrects the call/return stack based on the correction information stored therein, then for each valid one of the second plurality of entries, the control logic pops the top valid one of the second plurality of entries from the second stack.

An advantage of the present invention is that it enables invalidating events, such as detection of a branch instruction misprediction or exception, to be detected at multiple stages of the microprocessor pipeline while still enjoying the advantages of a call/return stack that remains consistent with main memory. It is advantageous to detect branch instruction mispredictions early in the pipeline, rather than only near the bottom of the pipeline, because it reduces pipeline bubbles by enabling correction of the misprediction and fetching of the correct instructions sooner than would be possible if the misprediction were detected only near the bottom of the pipeline.

Other features and advantages of the present invention will become apparent upon study of the remaining portions of the specification and drawings.